Remarks

Applicant thanks the Examiner for acknowledging the receipt of Preliminary Amendment dated 8/2/2001, change of address dated 06/26/2003, change in power of Attorney dated 09/02/2003, and drawings dated 11/17/2003. The Official Action rejected claims 1-40 and objected to claims 28, 34, and 39. Applicant has amended claims 25, 28, 31, 34, 37 and 39 and has canceled claims 26, 32 and 38. Claims 1-25, 27-31, 33-37 and 39-40 remain pending in the present application.

Claim Objections

The Official Action objected to claims 28, 34 and 39 because of informalities. In particular, the Official Action indicated that limitations of these claims directed to the error correction code memory and initializing the error correction code memory appeared to lack support in the specification. Applicant has amended claims 28, 34 and 39 to include the limitation "error checking and correction (ECC) memory" which is supported by at least paragraph [0028] of the present application. Furthermore, initializing ECC memory is support by at least paragraphs [0044]-[0063] of the present application. Applicant respectfully requests that the present objection of claims 28, 34 and 39 be withdrawn.

Claim Rejections – 35 USC § 103 (Collins/Levy)

The Official Action rejected claims 1, 3, 5-7, and 25-40 under 35 USC 103(a) as being unpatentable over Collins in view of Levy. Applicant has amended claims 25, 28, 31, 34, 37 and 39 and has canceled claims 26, 32 and 38. Applicant respectfully requests the rejection of claims 1, 3, 5-7, 25, 27-31, 33-37 and 39-40 be withdrawn.

Claims 1, 25, 31 and 37

Each of claims 1, 25, 31, and 37 require a processor with multiple logical processors or with a first logical processor and a second logical processor to execute initialization tasks. The Official Action indicates that Collins teaches using *two physical processors* to concurrently perform two initialization tasks before the OS receives control of the system. The Official Action indicates that Collins teaches using two physical processors in such a manner in order to reduce the booting time of the system. Since claims 1, 25, 31 and 37 require multiple logical processors and not multiple physical processors, the Official Action relies on Levy for a teaching of multiple logical processors. In particular, the Official Action indicates that Levy teaches a SMT processor that is capable of executing multiple threads concurrently and therefore teaches a processor having multiple logical processors. The Official Action further indicates that one skilled in the art would be motivated to replace the multiple processors of Collins with the SMT processor of Levy so as to further reduce the boot-up time of the Collins system.

However, one skilled in the art would not modify Collins in the proposed manner in order to reduce the boot-up time of the Collins system. An SMT processor such as the Levy may execute multiple threads but the multiple threads share at least some resources such as registers of the processor. As a result, the multiple threads contend for the shared resources and at times must wait for other threads to release shared resources before continuing. This contention for shared resources of the single processor means that, other things being equal, an SMT processor executes two simultaneous tasks slower than two physical processors. It should be noted that the Official Action appears to rely on Levy at column 10, lines 15-32 for the proposition that

a SMT processor system performs better than two and four processor multiprocessor systems. However, Levy actually states simulations show that an SMT processor achieves a speed-up over two and four-processor ***single-chip*** multiprocessors. In other words, Levy states a theoretical improvement over a single-chip multiprocessor having two or four processors but is silent in regard to comparisons to multiple physical processors such as for example the two physical processors of Collins.

Therefore, one skilled in the art would not be motivated to replace the two physical processors of Collins with the SMT processor of Levy because such a combination is likely to result in a system that takes longer to boot than the original Collins system due to the contention for shared resources in the SMT processor. Since there appears to be no motivation to make the proposed combination of Collins and Levy, the invention of claims 1, 25, 31 and 37 are not obvious in light of Collins and Levy. Applicant respectfully requests that the rejection of claims 1, 25, 31 and 37 be withdrawn.

Claims 3, 5-7, 27-30, 33-36 and 39-40

Each of claims 3, 5-7, 27-30, 33-36 and 39-40 includes one of claims 1, 25, 31 and 37 as a base claim. Accordingly, each of claims 3, 5-7, 27-30, 33-36 and 39-40 is allowable for at least the reasons stated above in regard to claims 1, 25, 31 and 37. Applicant respectfully requests that the rejection of claims 3, 5-7, 27-30, 33-36 and 39-40 be withdrawn.

Claim Rejections – 35 USC § 103 (Collins/Levy/Hobson)

The Official Action rejected claims 2, 12-13 and 15-17 under 35 USC 103(a) as being unpatentable over Collins and Levy in view of Hobson et al. (U.S. Patent

6,111,813). Applicant respectfully requests the rejection of claims 2, 12-13 and 15-17 be withdrawn.

Claim 12

Claim 12 requires a processor with multiple logical processors to execute initialization tasks. As indicated above, one skilled in the art would not be motivated to replace the two physical processors of Collins with the SMT processor of Levy because such a combination is likely to result in a system that takes longer to boot than the original Collin's system with two physical processors. Accordingly, there is no motivation to make the proposed combination of Collins, Levy and Hobson so as to arrive at the invention of claim 12. Applicant requests the rejection of claim 12 be withdrawn.

Claims 2, 13 and 15-17

Each of claims 2, 13 and 15-17 includes one of claims 1 and 12 as a base claim. Accordingly, each of claims 2, 13 and 15-17 is allowable for at least the reasons stated above in regard to claims 1 and 12. Applicant respectfully requests that the rejection of claims 2, 13 and 15-17 be withdrawn.

Claim Rejections – 35 USC § 103 (Collins/Levy/IPR)

The Official Action rejected claims 4, 8-11 and 22-24 under 35 USC 103(a) as being unpatentable over Collins and Levy in view of Intel Press Release (IPR) and corresponding Datasheet. Applicant respectfully requests the rejection of claims 4, 8-11 and 22-24 be withdrawn.

Claim 22

Claim 22 requires execution of initialization tasks by a Boot-Strap Logical Processor and a Alternate Logical Processor of a single physical processor. As indicated above, one skilled in the art would not be motivated to replace the two physical processors of Collins with the SMT processor of Levy. Accordingly, the proposed combination of Collins, Levy and the IPR is not obvious. Applicant respectfully requests the present rejection of claim 22 be withdrawn.

Claims 4, 8-11 and 23-24

Each of claims 4, 8-11 and 23-24 includes one of claims 1 and 22 as a base claim. Accordingly, each of claims 4, 8-11 and 23-24 is allowable for at least the reasons stated above in regard to claims 4, 8-11 and 23-24. Applicant respectfully requests that the rejection of claims 4, 8-11 and 23-24 be withdrawn.

Claim Rejections – 35 USC § 103 (Collins/Levy/Hobson/IPR)

The Official Action rejected claims 14 and 18-20 under 35 USC 103(a) as being unpatentable over Collins and Levy in view of Hobson, Intel Press Release (IPR) and corresponding Datasheet. Each of claims 14 and 18-20 includes claim 12 as a base claim. Accordingly, each of claims 14 and 18-20 is allowable for at least the reasons stated above in regard to claim 12. Applicant respectfully requests that the rejection of claims 14 and 18-20 be withdrawn.

Conclusion

The foregoing is submitted as a full and complete response to the Official Action. Applicant submits that the application is in condition for allowance. Reconsideration is requested, and allowance of the pending claims is earnestly solicited. Should it be determined that an additional fee is due under 37 CFR §§1.16 or 1.17, or any excess fee has been received, please charge that fee or credit the amount of overcharge to deposit account number 02-2666. If the Examiner believes that there are any informalities, which can be corrected by an Examiner's amendment, a telephone call to the undersigned at (503) 467-8778 is respectfully solicited.

Respectfully submitted,

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to MS Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313 on December 8, 2004.

By: _____ Date: December 8, 2004

Rachael Brown